Micromegas for EIC

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EIC R&D Review

ATTENTION

Proposal has changed significantly !

After further research and discussions

- retreat from plan to develop a lithography facility at MIT-Bates
- Tech-Etch can make most of what we require
- investigate alternative approaches to assembly and readout
- concentrate on optimizing micromegas design and performance

Budget request reduced by 261 k$!

Proposal text now has an addendum to this effect

Motivation

Micromegas very versatile and useful technology

- simple concept
- relatively easy and economical to produce
- applications in a variety of detectors
  - tracking, calorimetry, ...

We propose to leverage the experience and facilities at MIT

- spectrometers, wire chambers, GEMs, silicon strip, ...
- mechanical and electrical engineering
- machine shops, clean rooms, technicians, ...

Study and develop micromegas technology

- as resource for future detector development

Background

Micro-mesh gas structure → micromegas

- Y. Giomataris, CEA-Saclay, NIM, A376 (1996) 29–35.

Developed further

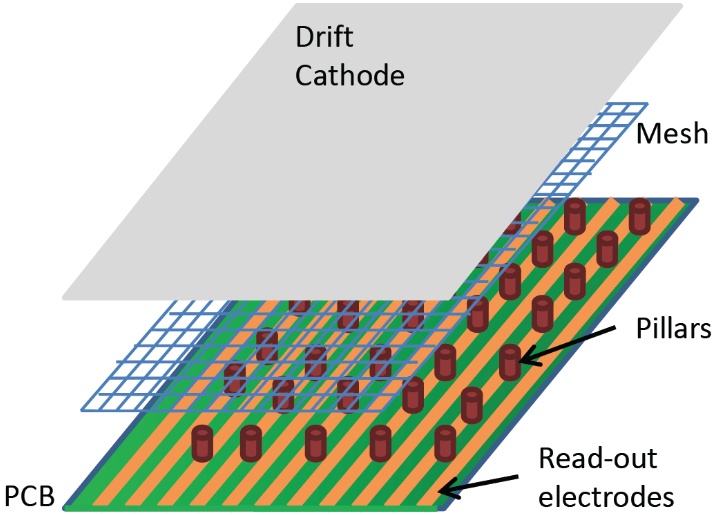
- CEA-Saclay
- CERN, RD51 Collaboration
- and elsewhere (generally in collaboration with Saclay or CERN)

Transfering “bulk” process to industry

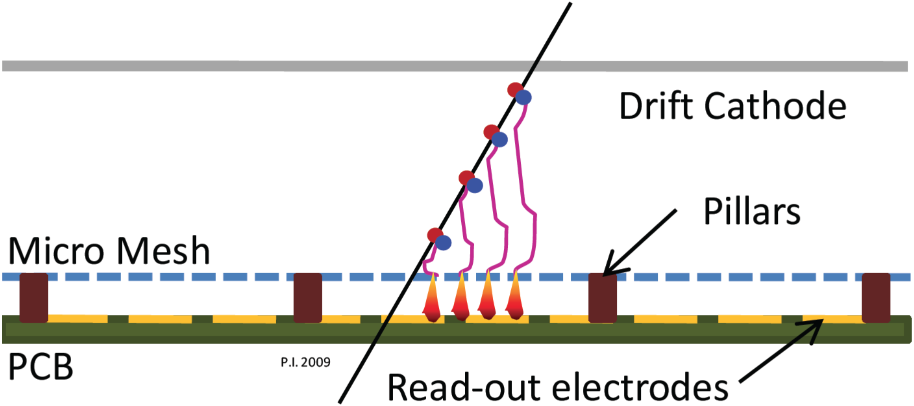
- Eltos, Somacis (Italy)
- Elvia (France)
- Triangle Labs (USA)

But detector design, innovation, assembly, and testing at research labs

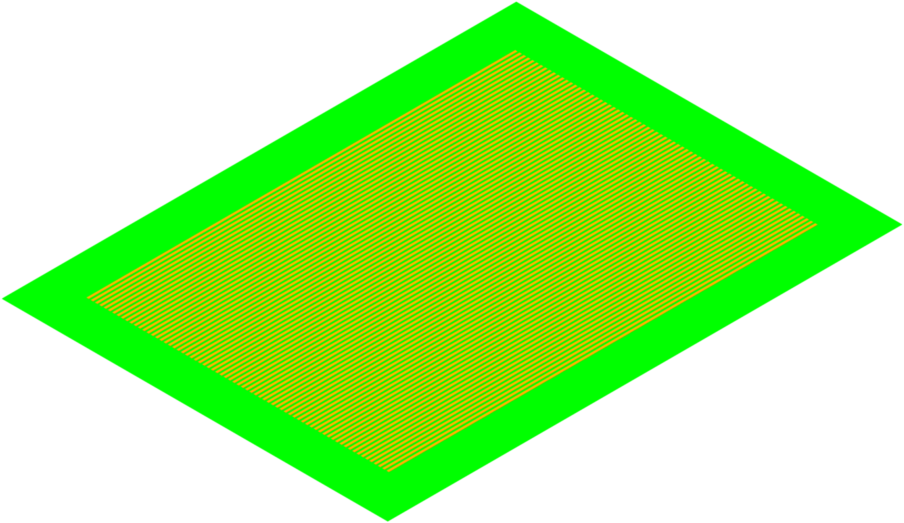
Basic Concept - Schematic



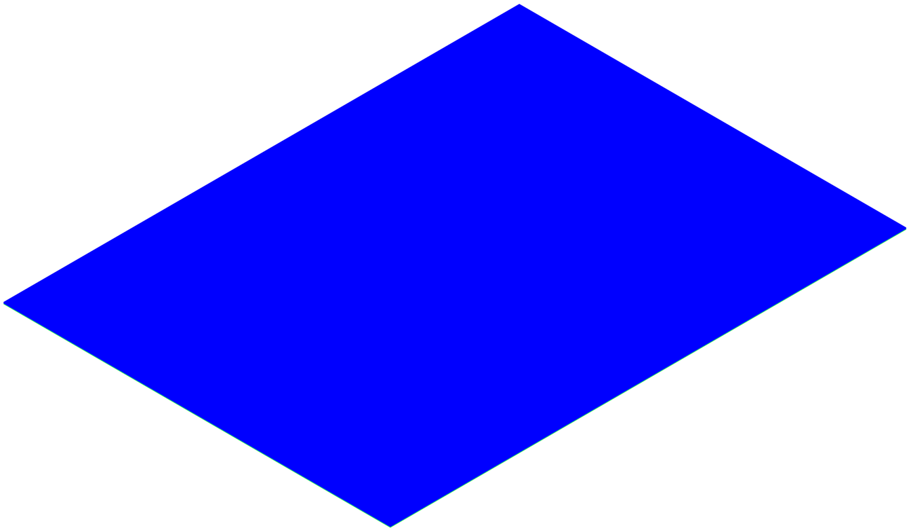
Basic Concept - Operation



Fabrication - PCB with readout pattern

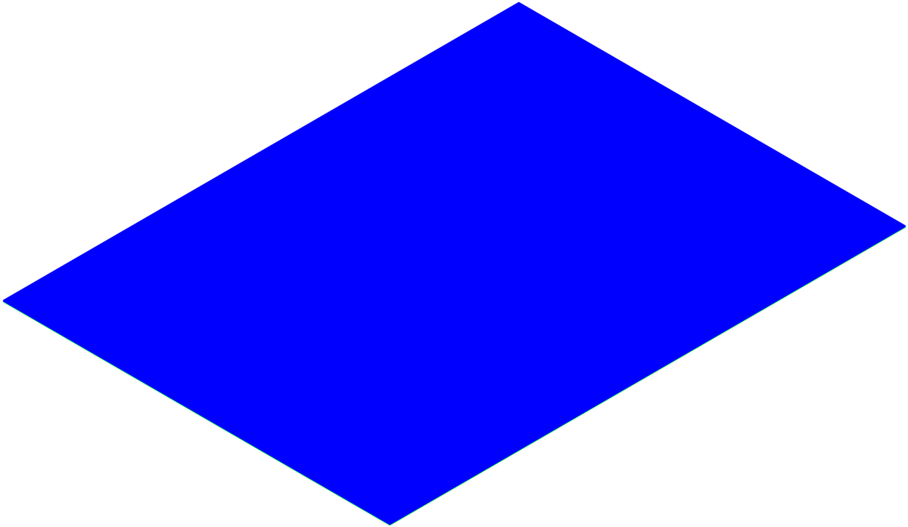


Fabrication - Laminate a layer of photoresist

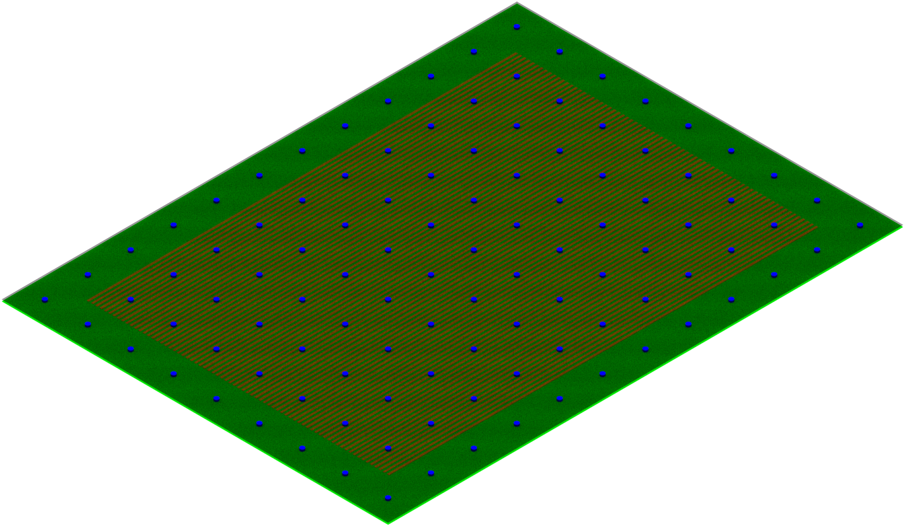


Fabrication - stretch wire mesh over photoresist

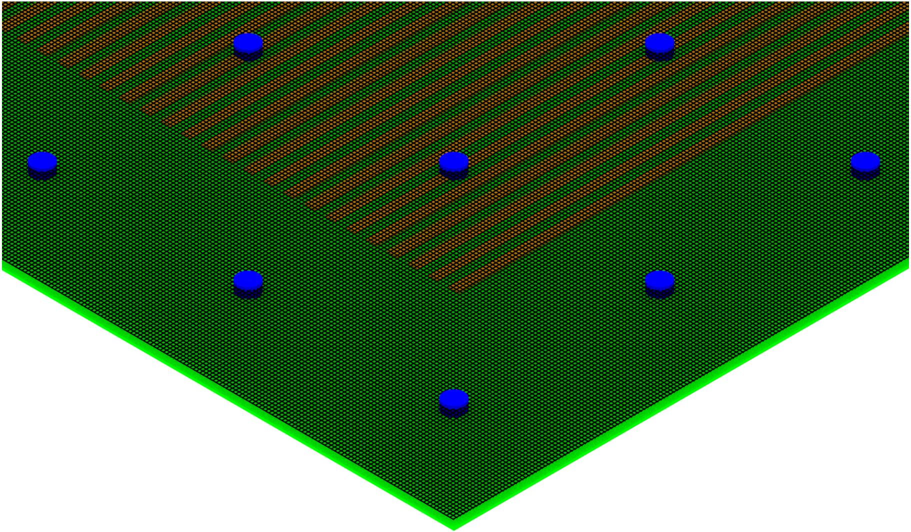
Fabrication - sandwich mesh with another photoresist layer



Fabrication - expose and develop pattern of pillars



Fabrication - Close-up



Fabrication

Easy to complete the detector

- install the PCB, pillar and mesh assembly into a gas enclosure
- attach cathode layer
- make HV and electronic connections
- test and install

Micromegas have many advantages

Impressions after M. Garçon talk and visiting Saclay

- physically thin ~ 3 mm (triple GEM ~ 9 mm)
- small radiation thickness $\sim 0.12\ X_0$ (triple GEM $\sim 0.23\ X_0$)
    - comparing micromegas mesh + gas to 3 GEM foils + gas
- gas gain similar to triple GEM
- excellent position resolution depending on the readout scheme
- readout scheme (PCB layout) can be tailored to detector needs
    - pad array, 1D lines, 2D lines+pads or crossed lines, stereo, XUV, etc.
- high rate, fast response (short distance for ion back-flow, ~ 100 ns)
- simple assembly, single layer
    - once PCB, pillar, and mesh ("bulk") assembly is produced
- possible to test "bulk" in air
- does not need especially clean environment
    - "bulk" can be cleaned and possibly repaired before detector assembly

Micromegas have some disadvantages

Production of the PCB, pillars, wire mesh or "bulk" is a critical step

- production of PCB is standard industrial technology, similar to GEM
- building pillars is also a standard industrial technology
- but incorporating wire mesh is not standard
- wire mesh must be smooth and a uniform distance from PCB
- needs a stretching frame (not a normal part in lithography)
    - this was motivation in initial proposal to develop a facility at MIT-Bates

Electrical breakdown can be a problem

- heavily ionizing particles or high rate
- damage PCB and/or readout electronics

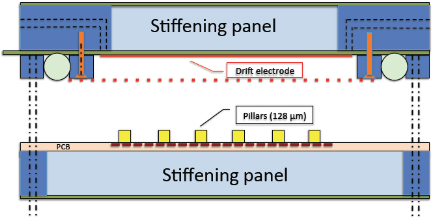
Avalanche is very localized

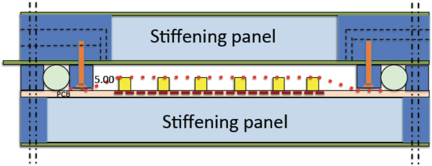
- depending on PCB design, may strike only a single readout line

Alternative approaches to support wire mesh

ATLAS upgrade for new "small" wheel uses micromegas detectors

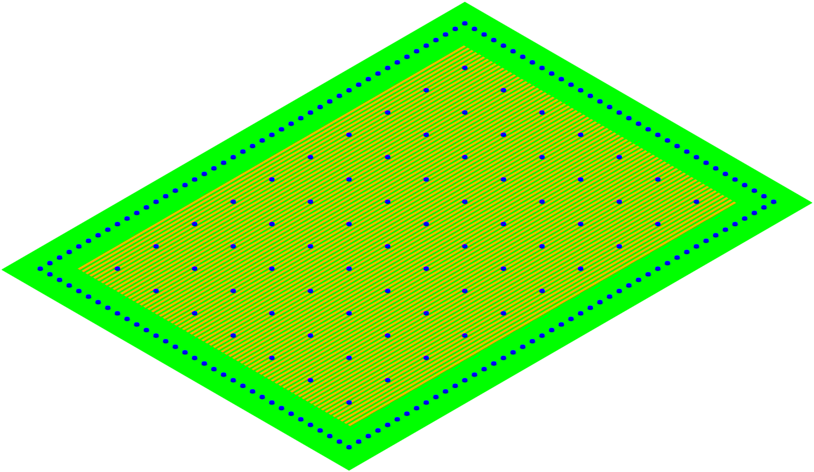
- PCB and pillars separate from mesh, standard lithographic process
- wire mesh connected to frame and pressed over pillars
- O-ring gas seal $\rightarrow$ can be taken apart, cleaned, fixed
- requires relatively wide frames, large dead area on smaller detectors





Another possibility to attach wire mesh

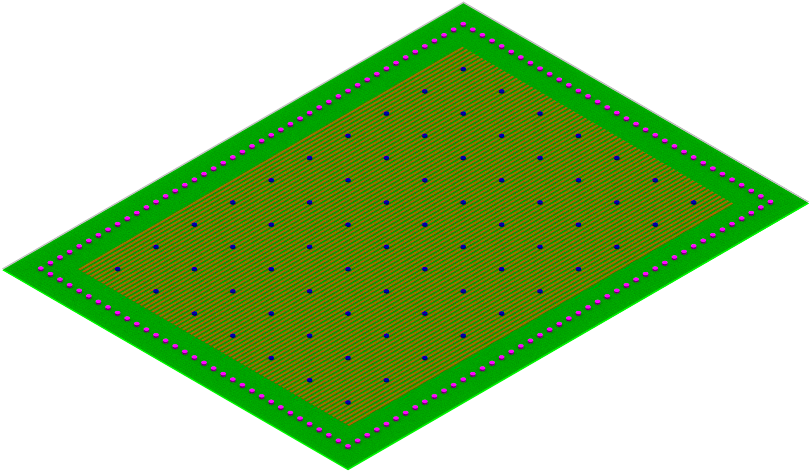
Produce PCB and pillars in standard lithographic process
- possibly with some extra pillars at edges



Another possibility to attach wire mesh

Stretch wire mesh over posts

- epoxy at edges and at some interior posts as necessary



Other ideas for supporting wire mesh

Attach pillars to wire mesh

- 3D printing
- glass beads
- . . .

Taking the wire mesh away from the “bulk” production

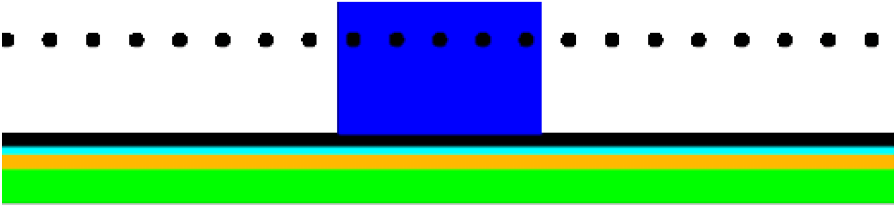
- simplifies the lithographic steps, any PCB manufacturer can do it
- opens up other possibilities

Handling electrical breakdown

Electrical breakdown can be mitigated by a resistive layer

- typically lines of resistive ink parallel to lines on PCB
- separated by dielectric
- capacitively coupled readout on parallel PCB line
- need resistance to be tens of megohm including terminating resistors
    - resistive line potential rises with discharge current to suppress discharge

Permits operating at higher gas gain



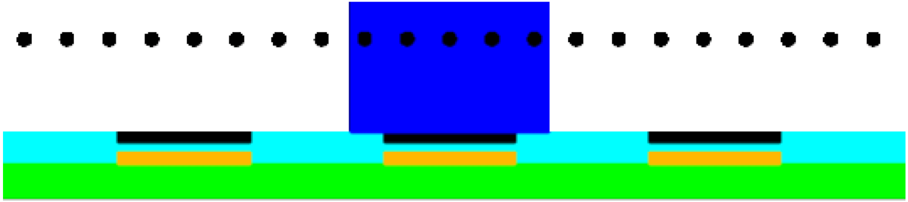
Production issues

Production of resistive lines involves non-standard lithographic procedures

- dielectric laminated over PCB - okay
- grooves etched in dielectric - okay
- resistive ink "dispensed" into grooves - ?
- pillars produced over resistive ink - ?

In operation the exposed dielectric charges up

- reduces gain, can take 10–15 minutes depending on rate



Resistive foils

There are standard resistive and capacitive foils used in PCB manufacture

- resistive layer (NiCr,NCAS, CrSiO) laminated to standard prepreg
- copper layer deposited over resistive layer
- etch copper to expose resistive layer
- commonly used to add an inline resistor in a PCB design
  - typical surface resistivity $25 - 1000\ \Omega/\square$
  - $100\ \mu$m wide line corresponds to $2.5 - 100\ \mathrm{k}\Omega/\mathrm{cm}$

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Resistance too low for breakdown protection on its own, but

- measure charge at both ends to determine position along length
- 2D readout with parallel lines, replace copper lines on PCB

Readout

Small gap means shower is very localized

- may only strike a single readout line of PCB
- micromegas often have very fine lines and pitches
  - okay if that resolution required
  - but a lot of channels to readout if not
- resistive layer useful here as well
  - protection from breakdown plus
  - spreads signal by capacitively coupling to neighboring lines

2D Readout

Micromegas can use the PCB readout schemes just like GEMs

- pads for high granularity
- parallel lines for 1D measurement
- designs with lines and pads, for 2D cartesian, stereo and XUV readout

Resistive layers are clearly useful

- but resistive lines couple to "all" perpendicular lines
- with high enough line resistance extent is limited

Rather than resistive lines use a complete resistive layer

- previous attempts had problems with uniformity in resistance
- resistive Kapton available with a range of resistances and uniformity
  - possible to apply this in standard lithographic procedure

Changes to budget request

No longer see a need for a lithography facility at MIT-Bates

Therefore, no need for:

- laminator
- exposure unit
- developer station
- special room and infrastructure
- manpower to set-up and maintain lithography facility

Also cutting back on travel

Adding XY table, controller, dispensers, etc.

- investigate alternative methods to support wire mesh
- dispensing resistive ink, ...
- capability for large area $(0.5 \times 2.0 \text{ m}^2)$ micromegas

Revised Budget

Item	2015	2016	2017
Equipment and consumables			
XY table, controller, dispensor	30.0 k$	30.0 k$	
PCBs, wire, foils, etc.	73.1 k$	91.4 k$	109.7 k$
Travel			
2 engineers, RD51 week	11.0 k$		
Manpower			
Engineer	0.2 FTE	0.2 FTE	0.2 FTE
	38.6 k$	39.8 k$	41.0 k$
Technician	0.2 FTE	0.2 FTE	0.2 FTE
	39.0 k$	40.2 k$	41.4 k$
Total	201.7 k$	201.4 k$	192.1 k$

Summary

Micromegas are an interesting technological option for future detectors

We want to leverage the experience and facilities at MIT to investigate:

- alternative means to support wire mesh,
- options for applying a resistive layer,
- different readout schemes, and
- develop the production of the base structure using standard lithographic procedures so the technology is more readily available.

Experience and technology as a resource for future EIC detectors

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Thank you